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Method To Reduce Stacking Fault Nucleation Sites And Reduce Forward Voltage Drift In Bipolar Devices

Abstract

A method is disclosed for preparing a substrate and epilayer for reducing stacking fault nucleation and reducing forward voltage (V_f) drift in silicon carbide-based bipolar devices. The method includes the steps of etching the surface of a silicon carbide substrate with a nonselective etch to remove both surface and subsurface damage, thereafter etching the same surface with a selective etch to thereby develop etch-generated structures from at least any basal plane dislocation reaching the substrate surface that will thereafter tend to either terminate or propagate as threading defects during subsequent epilayer growth on the substrate surface, and thereafter growing a first epitaxial layer of silicon carbide on the twice-etched surface.